CLAIMS:

Sub C1

1. A method of forming an isolation trench in a semiconductor comprising:

forming a first isolation trench portion having a first depth and having a first sidewall intersecting a surface of the semiconductor at a first angle;

forming a second isolation trench portion within and extending below the first isolation trench portion, the second isolation trench portion having a second depth and including a second sidewall intersecting the first sidewall at an angle with respect to the surface that is greater than the first angle; and

filling the first and second isolation trench portions with dielectric material.

2. The method of claim 1, wherein forming a second isolation trench portion includes forming the second angle to be between eighty and ninety degrees.

3. The method of claim 1, wherein forming a first isolation trench portion includes forming the first angle to be in a range of from about thirty degrees to about seventy degrees and forming a second isolation trench portion includes forming the second angle to be more than eighty degrees.

Sub Cont

4. The method of claim 1, wherein forming an isolation trench in a semiconductor comprises forming an isolation trench in silicon.

5. The method of claim 1, wherein forming a first isolation trench portion comprises:

forming a silicon nitride layer on the semiconductor surface;

forming a masking layer having an opening disposed therein atop the silicon nitride layer, the opening including sidewalls;

plasma etching through the silicon nitride layer using conditions that also deposit a polymer on the sidewalls;

continuing etching for a predetermined time interval after the silicon nitride layer has been broached and continuing to deposit polymer on the sidewalls; and

stopping the etching and depositing at the end of the predetermined time interval.

6. The method of claim 5, wherein etching and depositing comprises:

providing a mixture of gasses chosen from a group consisting of CF_4, CHF_3, CH_2F_2 and C_2F_8; and

supplying radio frequency excitation to the mixture.

Sub C Cont

7. The method of claim 5, wherein etching and depositing comprises:

providing fluorocarbon gases; and

supplying radio frequency excitation to the mixture.

8. The method of claim 1, wherein forming the first isolation trench portion comprises plasma etching the first isolation trench portion using gases including CF_4 and CHF_3 in a ratio of CF_4/CHF_3 = 0.11 to 0.67.

9. The method of claim 1, wherein forming the first isolation trench portion comprises:

forming a silicon nitride layer on the semiconductor surface;

forming a masking layer having an opening disposed therein atop the silicon nitride layer, the opening including sidewalls;

plasma etching through the silicon nitride layer using gases including CF_4 and CHF_3 in a ratio of CF_4/CHF_3 = 0.11 to 0.67;

depositing a polymer on the sidewalls during plasma etching;

continuing etching for a predetermined time after the silicon nitride layer has been broached and continuing depositing polymer on the sidewalls; and

stopping etching and depositing when the predetermined interval ends.

10. The method of claim 1, wherein forming a first isolation trench portion comprises forming a first isolation trench portion having a first depth of between five and fifty percent of a total trench depth.

11. The method of claim 1, further comprising planarizing the dielectric material filling the first and second isolation trench portions.

12. The method of claim 1, wherein forming a first isolation trench portion comprises forming a first isolation trench portion including a sidewall at least some of which forms a substantially straight linear segment.

13. A method of forming an isolation trench in a surface of a silicon wafer comprising:

forming a mask on the surface, the mask including an opening and sidewalls; and

etching the silicon surface using gases including CF_4 and CHF_3 in a ratio of CF_4/CHF_3 = 0.11 to 0.67 to form a first isolation trench portion.

14. The method of claim 13, wherein etching the silicon surface includes forming a first isolation trench portion having a first sidewall that intersects the silicon surface at an angle in a range of from about thirty degrees to about seventy degrees.

15. The method of claim 14, wherein forming a first isolation trench portion comprises forming a first isolation trench portion including a sidewall at least some of which forms a substantially straight linear segment.

16. The method of claim 13, further comprising forming a second isolation trench portion within and extending below the first isolation trench portion, the second isolation trench portion including a second sidewall intersecting the first sidewall at an angle with respect to the surface that is greater than the first angle.

17. The method of claim 16, wherein forming a first isolation trench portion comprises forming a first isolation trench portion having a first depth of between five and fifty percent of a total trench depth.

18. The method of claim 17, further comprising:

filling the first and second isolation trench portions with dielectric material; and

planarizing the dielectric material filling the first and second isolation trench portions.

19. The method of claim 13, wherein forming a mask comprises:

forming a silicon nitride layer on the semiconductor surface; and

forming a masking layer having an opening disposed therein atop the silicon nitride layer, the opening including sidewalls.

20. The method of claim 19, wherein etching the surface comprises:

plasma etching through the silicon nitride layer;

continuing etching for a predetermined time interval after the silicon nitride layer has been broached and continuing to deposit polymer on the sidewalls; and

stopping the etching and depositing at the end of the predetermined time interval.

21. The method of claim 19, further comprising forming a second isolation trench portion within and extending below the first isolation trench portion, the second isolation trench portion having a second depth and including a second sidewall intersecting the first sidewall at an angle with respect to the surface that is greater than the first angle.

22. A method of forming an isolation trench-isolated transistor comprising:

forming first and second isolation trenches disposed to a respective side of a portion of silicon, forming the first and second isolation trenches comprising:

forming a mask on the surface, the mask including first and second openings corresponding to the first and second isolation trenches;

forming a first isolation trench portion in each of the first and second openings, each first isolation trench portion having a first depth and having a first sidewall intersecting a surface of the semiconductor at a first angle; and

forming a second isolation trench portion within and extending below each of the first isolation trench portions, the second isolation trench portions having a second depth and including a second sidewall intersecting a respective one of the first sidewalls at an angle with respect to the surface that is greater than the first angle; the method further comprising:

filling the first and second isolation trench portions with dielectric material;

forming a gate extending across the silicon portion from the first isolation trench to the second isolation trench; and

forming source and drain regions extending between the first and

second isolation trench portions, the source region being disposed adjacent one side of the gate and the drain region being disposed adjacent another side of the gate that is opposed to the one side.

23. The method of claim 22, wherein forming a first isolation trench portion comprises etching the silicon surface using gases including CF_4 and CHF_3 in a ratio of CF_4/CHF_3 = 0.11 to 0.67.

24. The method of claim 22, wherein forming a mask comprises:

forming a silicon nitride layer on the semiconductor surface; and

forming a masking layer having an opening disposed therein atop the silicon nitride layer, the opening including sidewalls.

25. The method of claim 22, wherein forming a first isolation trench portion comprises:

plasma etching through the silicon nitride layer using conditions that also deposit a polymer on the sidewalls;

continuing etching for a predetermined time after the silicon nitride layer has been broached and continuing to deposit polymer on the sidewalls; and

stopping the etching and depositing at the end of the predetermined interval.

26. The method of claim 25, wherein plasma etching comprises etching using gases including CF_4 and CHF_3 in a ratio of CF_4/CHF_3 = 0.11 to 0.67.

27. The method of claim 22, wherein forming a first isolation trench portion comprises forming a first isolation trench portion having a first sidewall intersecting a surface of the semiconductor at an angle in a range of from about thirty degrees to about seventy degrees.

28. The method of claim 22, wherein forming a first isolation trench portion comprises forming a first isolation trench portion including a sidewall at least some of which forms a substantially straight linear segment.

29. The method of claim 27, wherein forming a second isolation trench portion comprises forming a second isolation trench portion having a second sidewall forming an angle of more than eighty degrees with the surface.

30. The method of claim 22, wherein forming a first isolation trench portion comprises forming a first isolation trench portion having a first depth of between five and fifty percent of a total trench depth.

31. The method of claim 30, further comprising planarizing the dielectric material filling the first and second isolation trench portions.

32. The method of claim 22, wherein forming a gate comprises forming a gate comprising polysilicon.

33. A trench-isolated transistor comprising:

first and second isolation trenches each disposed on a respective side of a portion of silicon, the first and second isolation trenches each comprising:

a first isolation trench portion having a first depth and having a first sidewall intersecting a surface of the silicon at a first angle;

a second isolation trench portion within and extending below the first isolation trench portion, the second isolation trench portion having a second depth and including a second sidewall intersecting the first sidewall at an angle with respect to the surface that is greater than the first angle; and

a dielectric material filling the first and second isolation trench portions, the transistor further comprising:

a gate extending across the silicon portion from the first isolation trench to the second isolation trench; and

source and drain regions extending between the first and second isolation trench portions and across the silicon portion, the source region being disposed adjacent one side of the gate and the drain region being disposed adjacent another side of the gate that is opposed to the one side.

34. The trench-isolated transistor of claim 33, wherein the first isolation trench portion comprises a sidewall at least some of which forms a substantially straight linear segment.

35. The trench-isolated transistor of claim 33, wherein the second angle is between eighty and ninety degrees.

36. The trench-isolated transistor of claim 33, wherein the first angle is in a range of from about thirty degrees to about seventy degrees and the second angle is more than eighty degrees.

37. The trench-isolated transistor of claim 33, wherein the first isolation trench portion has a first depth of between five and fifty percent of a total trench depth.

38. The trench-isolated transistor of claim 33, wherein the dielectric material filling the first and second isolation trench portions has a planar surface.

39. The trench-isolated transistor of claim 33, wherein the first angle is in a range of from about thirty degrees to about seventy degrees.

40. The trench-isolated transistor of claim 39, wherein the second angle is in a range of from eighty to ninety degrees.

41. The trench-isolated transistor of claim 33, wherein the transistor is formed as a part of a memory integrated circuit.

42. A trench isolation structure formed in a semiconductor comprising:

a first isolation trench portion having a first depth and having a first sidewall intersecting a surface of the semiconductor at a first angle;

a second isolation trench portion within and extending below the first isolation trench portion, the second isolation trench portion having a second depth and including a second sidewall intersecting the first sidewall at an angle with respect to the surface that is greater than the first angle; and

a dielectric material filling the first and second isolation trench portions.

43. The trench isolation structure of claim 42, wherein the first isolation trench portion comprises a sidewall at least some of which forms a substantially straight linear segment.

44. The trench isolation structure of claim 42, wherein the first angle is in a range of from about thirty degrees to about seventy degrees and the second angle is more than eighty degrees.

45. The trench isolation structure of claim 42, wherein the first angle is in a range of from about thirty degrees to about seventy degrees.

46. The trench isolation structure of claim 42, wherein the first isolation trench portion has a first depth of between five and fifty percent of a total trench depth.

47. The trench isolation structure of claim 42, wherein the trench isolation structure is formed in a memory integrated circuit.

48. A memory cell including:

a capacitor;

a trench-isolated transistor having a gate, a drain and a source, the source being coupled to one terminal of the capacitor, the trench-isolated transistor including:

first and second isolation trenches each disposed on a respective side of a portion of silicon, the first and second isolation trenches each comprising:

a first isolation trench portion having a first depth and having a first sidewall intersecting a surface of the silicon at a first angle;

a second isolation trench portion within and extending below the first isolation trench portion, the second isolation trench portion having a second depth and including a second sidewall intersecting the first sidewall at an angle with respect to the surface that is greater than the first angle; and

a dielectric material filling the first and second isolation trench portions;

the transistor further comprising:

a gate extending across the silicon portion from the first isolation trench to the second isolation trench; and

source and drain regions extending between the first and second isolation trench portions and across the silicon portion, the

source region being disposed adjacent one side of the gate and the drain region being disposed adjacent another side of the gate that is opposed to the one side;

the memory cell further including:

a bitline coupled to the drain; and

a wordline coupled to the gate.

49. The memory cell of claim 48, wherein the gate comprises polysilicon.

50. The memory cell of claim 48, wherein the first isolation trench portion comprises a sidewall at least some of which forms a substantially straight linear segment.

51. The memory cell of claim 48, wherein the first angle is in a range of from about thirty degrees to about seventy degrees and the second angle is more than eighty degrees.

52. The memory cell of claim 48, wherein the first angle is in a range of from about thirty degrees to about seventy degrees.

53. The memory cell of claim 48, wherein the first isolation trench portion has a first depth of between five and fifty percent of a total trench depth.

54. The memory cell of claim 48, wherein the memory cell is included within a DRAM integrated circuit.

55. A DRAM comprising:

address decoding circuitry;

a group of bitlines coupled to the address decoding circuitry and extending in a first direction;

a group of wordlines coupled to the address decoding circuitry and extending in a second direction, each wordline in the group of wordlines intersecting each of the bitlines in the group of bitlines once at an intersection;

a plurality of memory cells each disposed at one of the intersections, each memory cell comprising:

a capacitor;

a trench-isolated transistor having a gate, a drain and a source, the source being coupled to one terminal of the capacitor, the trench-isolated transistor including:

first and second isolation trenches each disposed on a respective side of a portion of silicon, the first and second isolation trenches each comprising:

a first isolation trench portion having a first depth and having a first sidewall intersecting a surface of the silicon at a first angle;

a second isolation trench portion within and extending below the first isolation trench portion, the second isolation trench portion having a second depth and including a second

sidewall intersecting the first sidewall at an angle with respect to the surface that is greater than the first angle; and

a dielectric material filling the first and second isolation trench portions;

the transistor further comprising:

a gate extending across the silicon portion from the first isolation trench to the second isolation trench; and

source and drain regions extending between the first and second isolation trench portions and across the silicon portion, the source region being disposed adjacent one side of the gate and the drain region being disposed adjacent another side of the gate that is opposed to the one side;

each memory cell further including:

one bitline of the group of bitlines coupled to the drain; and

one wordline of the group of wordlines coupled to the gate.

56. The DRAM of claim 55, wherein the first isolation trench portion comprises a sidewall at least some of which forms a substantially straight linear segment.

57. The DRAM of claim 55, wherein the gate comprises polysilicon.

58. The DRAM of claim 55, wherein the first angle is in a range of from about thirty degrees to about seventy degrees and the second angle is more than eighty degrees.

59. The DRAM of claim 55, wherein the first angle is in a range of from about thirty degrees to about seventy degrees.

60. The DRAM of claim 55, wherein the first isolation trench portion has a first depth of between five and fifty percent of a total trench depth.

61. The DRAM of claim 55, wherein the dielectric material filling the first and second isolation trench portions includes a planar outer surface.

add C27